FIG. 1

FIG. 2

START

PLACE PROCESSOR CORE IN TEST MODE ⌐21

GENERATE ONE OR MORE PSEUDO-RANDOM/DETERMINISTIC TEST VECTORS FOR PERIPHERAL DEVICES USING MISSION DATA PATHS OF PROCESSOR CORE, PROVIDE THE TEST VICTORS TO SCAN CHAINS, RECOVER PRE-TEST STATE OF SCAN CHAINS OR TEST RESPONSES TO THE PRIOR SET OF TEST VECTORS AND COMPACTING THE TEST RESPONSES AS THEY ARE RECOVERED ⌐22

APPLY TEST VECTORS TO PERIPHERAL DEVICES, STORING TEST RESPONSES INTO SCAN CHAINS ⌐23

NO ◇ DONE ? ⌐24

YES

RESTORE SAVED STATE OF SCAN CHAINS, RECOVER TEST RESPONSES TO LAST SET OF TEST VECTORS, COMPACTING TEST RESPONSES AS THEY ARE RECOVERED ⌐25
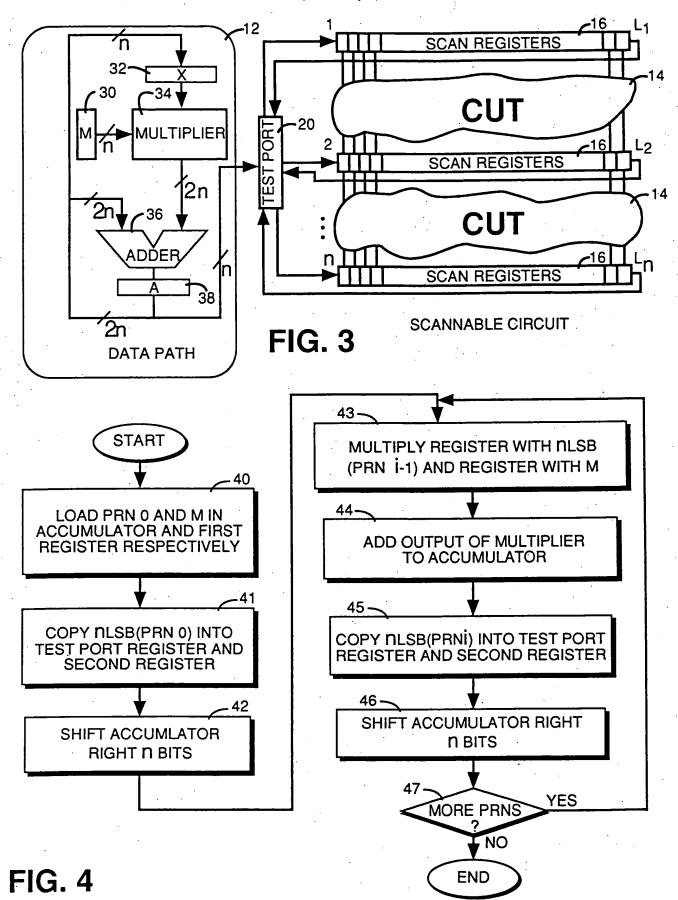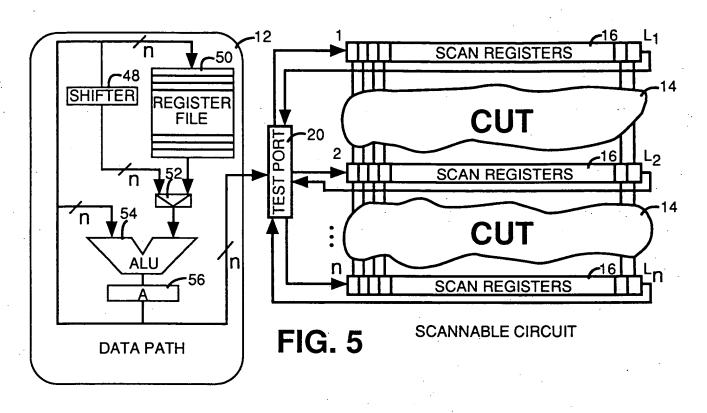
END

FIG. 3

FIG. 4

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SCAN-BASED INTEGRATED CIRCUITS
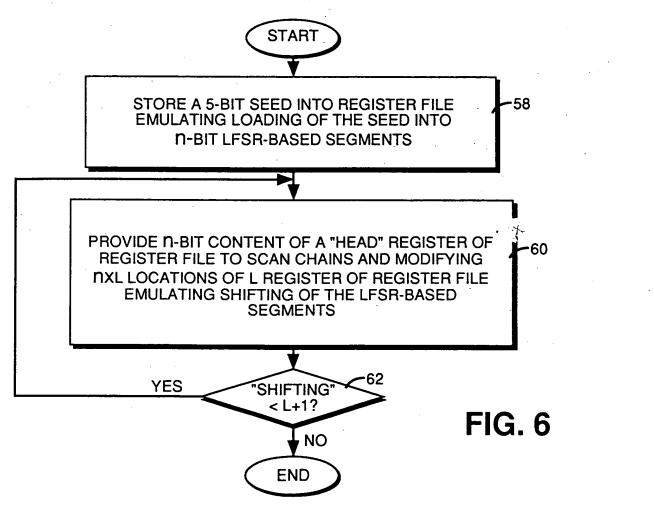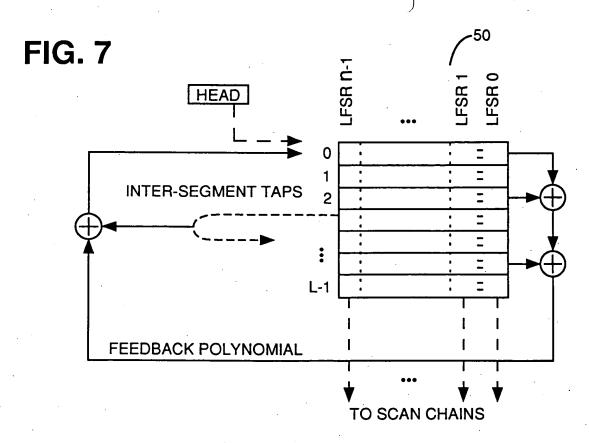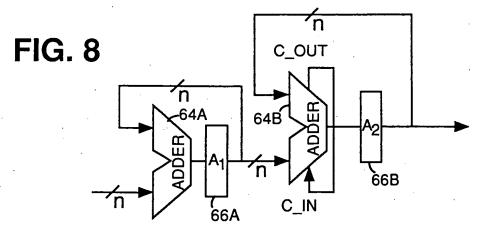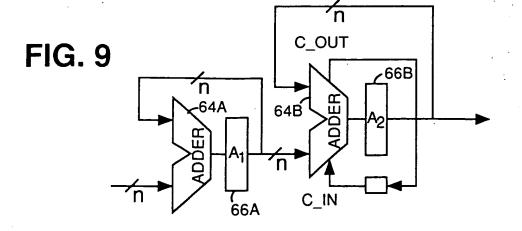Inventor(s): Rajski et al.
Express Mail Label No. EV175409692US
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FIG. 5

FIG. 6

FIG. 7

FIG. 8

FIG. 9

FIG. 10

START

MOVE NEXT TEST RESPONSE
TO FIRST AND SECOND
STAGE ACCUMULATORS — 74

ADD TEST RESPONSE TO
SIGNATURE AT FIRST STAGE,
CASCADE RESULT, THEN
ADD TEST RESPONSE AGAIN
AT SECOND STAGE — 76

MORE
TEST RESPONSES
?

YES

NO

END

FIG. 11

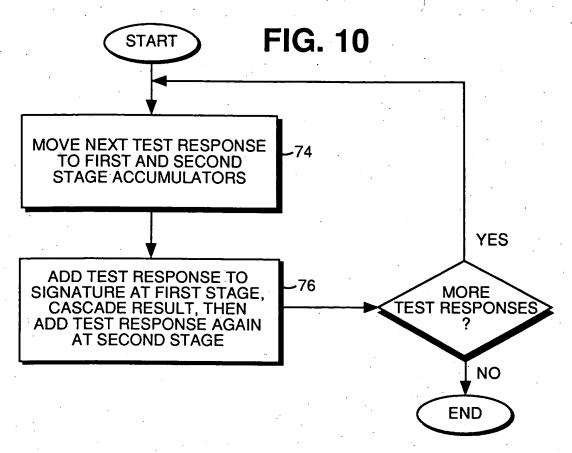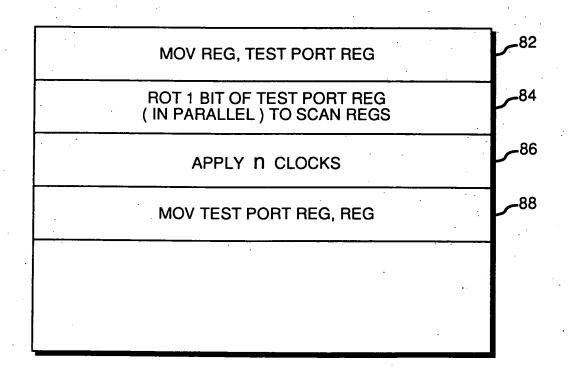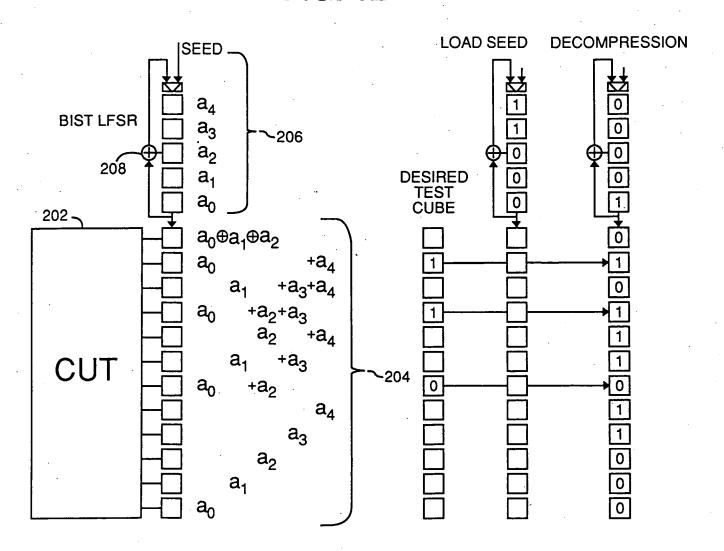| MOV REG, TEST PORT REG | — 82 |
ROT 1 BIT OF TEST PORT REG (IN PARALLEL) TO SCAN REGS	— 84
APPLY n CLOCKS	— 86
MOV TEST PORT REG, REG	— 88

FIG. 12

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SCAN-BASED INTEGRATED CIRCUITS
Inventor(s): Rajski et al.
Express Mail Label No. EV175409692US
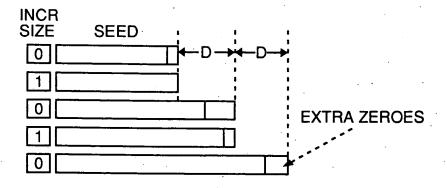Date of Deposit: February 10, 2004

FIG. 13

FIG. 14